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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/924,185	08/02/2001	Michael Holtzman	M-10246 US	2657

36257 7590 01/12/2005

PARSONS HSUE & DE RUNTZ LLP
655 MONTGOMERY STREET
SUITE 1800
SAN FRANCISCO, CA 94111

EXAMINER	
CLEARY, THOMAS J	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 01/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/924,185	HOLTZMAN ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on th cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-62* is/are pending in the application.

4a) Of the above claim(s) *56-62* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 August 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20020924, 20030122*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-25 and 39-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claims 1 and 13 recite the limitation "the processor" in Line 9 of Claim 1 and Line 9 of Claim 13. There is insufficient antecedent basis for this limitation in the claim. It is unclear whether "the processor" is meant to refer to the processing system of the processing unit.

4. Claim 11 recites the limitation "through the using the system data" in Line 3. It is unclear as to what this refers to.

5. Claim 19 recites the limitation "prerecorded continuous media" in Line 2. It is unclear as to what the continuous media is recorded prior to.

6. Claims 21, 23, and 24 recite the limitation "said at least one operating sequence" in Lines 1-2 of Claim 21, Lines 1-2 of Claim 23, and Lines 1-2 of Claim 24. There is insufficient antecedent basis for this limitation in the claim. It is unclear as to whether "said at least one operating sequence" is the same sequence as the "operating sequence" of Claim 13.

7. Claim 39 recites the limitation "wherein said processing is compressing" on Lines 2-3. It is unclear as to how data stored in compressed form is further compressed. Based on the similarity of Claim 39 to Claim 30, the Examiner will assume that the limitation should read "wherein said processing is decompressing" for the purposes of examination.

8. Claim 40 recites the limitation "wherein said processing is encrypting" on Line 2. It is unclear as to how data stored in encrypted form is further encrypted. Based on the similarity of Claim 40 to Claim 32, the Examiner will assume that the limitation should read "wherein said processing is decrypting" for the purposes of examination.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1, 2, 3, 8, 10, 11, 12, 13, 14, 15, 16, 23, 25 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 5,923,884 to Peyret et al. ("Peyret").

11. In reference to Claim 1, Peyret discloses an add-on card (See Figure 1 Number 20) for detachably coupling to a processing system (See Figure 4) comprising: an interface for communicating with said processing system while said add-on card is coupled with said processing system (See Figure 4 Number 86); a program storage memory storing at least one operating sequence (See Figure 1 Number 26 and Column 4 Line 67 – Column 5 Line 2); a mass storage memory including a program memory portion storing at least one additional operating sequence (See Figure 1 Number 30 and Column 5 Lines 7-11); and a processing unit coupled to said interface, said program storage memory, and said mass storage memory, whereby the processor can operate on data transferred between the card and the processing system through the interface according to said at least one additional operating sequence (See Figures 1 and 4 Number 22 and Column 5 Lines 13-35).

12. In reference to Claim 2, Peyret discloses the limitations as applied to Claim 1 above. Peyret further discloses a card bus whereby the processing unit, the interface

and the program storage memory are connected (See Figure 1); and a mass storage interface by which the mass storage memory is connected to the card bus (See Figure 1).

13. In reference to Claim 3, Peyret discloses the limitations as applied to Claim 2 above. Peyret further discloses that the mass storage is a flash memory (See Column 4 Lines 63-67) which is a non-linear memory. Thus, the mass storage interface is inherently a non-linear interface.

14. In reference to Claim 8, Peyret discloses the limitations as applied to Claim 1 above. Peyret further discloses that at least one additional operating sequence includes a data encryption/decryption routine (See Column 5 Lines 27-34).

15. In reference to Claim 10, Peyret discloses the limitations as applied to Claim 1 above. Peyret further discloses that the mass storage memory is a flash memory (See Column 4 Lines 63-67).

16. In reference to Claim 11, Peyret discloses the limitations as applied to Claim 1 above. Peyret further discloses that the mass storage memory further includes a portion storing system data, whereby the processor can operate on data transferred between the card and the processing system through the use of the system data (See Column 5 Lines 7-11 and Column 5 Line 36 – Column 6 Line 65).

17. In reference to Claim 12, Peyret discloses the limitations as applied to Claim 1 above. Peyret further discloses that the mass storage further includes a portion for storing user data (See Column 7 Lines 33-67).

18. In reference to Claim 13, Peyret discloses an add-on card (See Figure 1 Number 20) for detachably coupling to a processing system (See Figure 4) comprising: an interface for communicating with said processing system while said add-on card is coupled with said processing system (See Figure 4 Number 86); a program storage memory storing an operating sequence (See Figure 1 Number 26 and Column 4 Line 67 – Column 5 Line 2); a processing unit coupled to said interface and said program storage memory (See Figures 1 and 4 Number 22); and a mass storage memory coupled to said processing unit, whereby the processor can operate on data transferred between the interface and the mass storage memory according to said operating sequence (See Figures 1 and 4 Number 30 and Column 5 Lines 13-35).

19. In reference to Claim 14, Peyret discloses the limitations as applied to Claim 13 above. Peyret further discloses a card bus whereby the processing unit, the interface and the program storage memory are connected (See Figure 1); and a mass storage interface by which the mass storage memory is connected to the card bus (See Figure 1).

20. In reference to Claim 15, Peyret discloses the limitations as applied to Claim 14 above. Peyret further discloses that the mass storage is a flash memory (See Column 4 Lines 63-67) which is a non-linear memory. Thus, the mass storage interface is inherently a non-linear interface.

21. In reference to Claim 16, Peyret discloses the limitations as applied to Claim 13 above. Peyret further discloses that the mass storage memory includes a program memory portion storing at least one additional operating sequence (See Figure 1 Number 30 and Column 5 Lines 7-11).

22. In reference to Claim 23, Peyret discloses the limitations as applied to Claim 13 above. Peyret further discloses that at least one operating sequence includes a data encryption/decryption routine (See Column 5 Lines 27-34).

23. In reference to Claim 25, Peyret discloses the limitations as applied to Claim 13 above. Peyret further discloses that the mass storage memory is a flash memory (See Column 4 Lines 63-67).

24. Claims 4 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Peyret and The Free On-Line Dictionary of Computing ("FOLDOC").

25. In reference to Claim 4, Peyret discloses the limitations as applied to Claim 1 above. The data transferred between the host and the add on card is inherently sent in a continuous (streaming) fashion, as evidenced by FOLDOC, which defines a stream as any flow of data from a sender to a single receiver (See 'stream').

26. In reference to Claim 17, Peyret discloses the limitations as applied to Claim 13 above. The data transferred between the host and the add on card is inherently sent in a continuous (streaming) fashion, as evidenced by FOLDOC, which defines a stream as any flow of data from a sender to a single receiver (See 'stream').

27. In reference to Claim 19, Peyret and FOLDOC disclose the limitations as applied to Claim 17 above. Peyret further discloses that the mass-storage memory contains prerecorded media (See Column 5 Lines 7-12 and Column 6 Lines 28-44).

28. Claims 1, 13, 26, and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by European Patent Application Publication Number 0 292 248 to Steiner et al. ("Steiner").

29. In reference to Claim 1, Steiner discloses an add-on card for detachably coupling to a processing system (See Figure 1 and Column 1 Lines 3-26) comprising: an interface for communicating with said processing system while said add-on card is coupled with said processing system (See Column 1 Lines 51-54); a program storage

memory storing at least one operating sequence (See Column 1 Line 61 – Column 2 Line 8); a mass storage memory including a program memory portion storing at least one additional operating sequence (See Column 1 Lines 44-50); and a processing unit coupled to said interface, said program storage memory, and said mass storage memory, whereby the processor can operate on data transferred between the card and the processing system through the interface according to said at least one additional operating sequence (Column 1 Lines 3-11).

30. In reference to Claim 13, Steiner discloses an add-on card for detachably coupling to a processing system (See Figure 1 and Column 1 Lines 3-26) comprising: an interface for communicating with said processing system while said add-on card is coupled with said processing system (See Column 1 Lines 51-54); a program storage memory storing an operating sequence (See Column 1 Line 61 – Column 2 Line 8); a processing unit coupled to said interface and said program storage memory (Column 1 Lines 3-11); and a mass storage memory coupled to said processing unit, whereby the processor can operate on data transferred between the interface and the mass storage memory according to said operating sequence (See Column 1 Lines 44-50).

31. In reference to Claim 26, Steiner discloses providing an add-on card (See Figure 1 and Column 1 Lines 3-26) with a processing unit (Column 1 Lines 3-11) and a non-volatile mass storage memory (See Column 1 Lines 44-50); causing the add-on card to be attached to the host system (See Column 1 Lines 51-54); processing data stored in

the mass storage memory with the processing unit (See Column 3 Lines 38-44); and supplying the processed data to host (See Column 4 Lines 3-8).

32. In reference to Claim 34, Steiner discloses the limitations as applied to Claim 26 above. Steiner further discloses downloading an application from the host to the add-on card subsequent to said causing the add-on card to be attached to the host system, wherein said processing is performed according to the downloaded application (See Column 1 Lines 27-50).

33. In reference to Claim 36, Steiner discloses providing an add-on card (See Figure 1 and Column 1 Lines 3-26) with a processing unit (Column 1 Lines 3-11) and a non-volatile mass storage memory (See Column 1 Lines 44-50); causing the add-on card to be attached to the host system (See Column 1 Lines 51-54); supplying data from the host to the add-on card (See Column 3 Lines 32-36); processing data supplied from the host with the processing unit (See Column 3 Lines 38-44); and storing the processed data in the mass storage memory (See Column 4 Lines 3-8).

34. In reference to Claim 42, Steiner discloses the limitations as applied to Claim 36 above. Steiner further discloses downloading an application from the host to the add-on card subsequent to said causing the add-on card to be attached to the host system, wherein said processing is performed according to the downloaded application (See Column 1 Lines 27-50).

35. Claims 1, 9, 13, 24, 43, and 50 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 5,987,155 to Dunn et al. ("Dunn").

36. In reference to Claim 1, Dunn discloses an add-on card (See Figure 2 Number 25) for detachably coupling to a processing system (See Figure 2 Number 20) comprising: an interface for communicating with said processing system while said add-on card is coupled with said processing system (See Column 7 Lines 27-29); a program storage memory storing at least one operating sequence (See Column 3 Lines 22-28); a mass storage memory including a program memory portion storing at least one additional operating sequence (See Column 3 Lines 22-28); and a processing unit coupled to said interface, said program storage memory, and said mass storage memory, whereby the processor can operate on data transferred between the card and the processing system through the interface according to said at least one additional operating sequence (See Column 3 Lines 22-28 and Column 7 Lines 31-37).

37. In reference to Claim 9, Dunn discloses the limitations as applied to Claim 1 above. Dunn further discloses that said at least one additional operating sequence includes a voice recognition program (See Column 6 Lines 8-40).

38. In reference to Claim 13, Dunn discloses an add-on card (See Figure 2 Number 25) for detachably coupling to a processing system (See Figure 2 Number 20)

comprising: an interface for communicating with said processing system while said add-on card is coupled with said processing system (See Column 7 Lines 27-29); a program storage memory storing an operating sequence (See Column 3 Lines 22-28); a processing unit coupled to said interface and to said program storage memory (See Column 3 Lines 22-28); a mass storage memory coupled to said processing unit (See Column 3 Lines 22-28), whereby the processor can operate on data transferred between the interface and the mass storage memory according to said operating sequence (See Column 3 Lines 22-28 and Column 7 Lines 31-37).

39. In reference to Claim 9, Dunn discloses the limitations as applied to Claim 1 above. Dunn further discloses that said at least one operating sequence includes a voice recognition program (See Column 6 Lines 8-40).

40. In reference to Claim 43, Dunn discloses providing an add-on card (See Figure 2 Number 25) including a processing unit and a non-volatile mass storage memory (See Column 3 Lines 22-28), wherein the mass storage memory includes a program memory portion in which are stored a plurality of applications (See Column 3 Lines 22-28); coupling the add-on card to the host system (See Column 7 Lines 27-29); causing one of the applications to be selected; receiving data from the host on the add-on card (See Column 7 Lines 31-32); processing data received from the host with the processing unit according to the selected application (See Column 7 Lines 31-37); and supplying the processed data to host (See Column 7 Lines 32-35).

41. In reference to Claim 50, Dunn discloses the limitations as applied to Claim 43 above. Dunn further discloses that the selected application is voice recognition (See Column 6 Lines 8-40).

42. Claims 13, 22, 26, and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 5,995,018 to Hane et al. ("Hane").

43. In reference to Claim 13, Hane discloses an add-on card (See Figure 1 Number 1) for detachably coupling to a processing system (See Figure 1 Number 2) comprising: an interface for communicating with said processing system while said add-on card is coupled with said processing system (See Figure 1 Number 8); a processing unit (See Figure 1 Number 10) which inherently includes a program storage memory storing an operating sequence; and a mass storage memory coupled to said processing unit (See Figure 1 Number 11), whereby the processor can operate on data transferred between the interface and the mass storage memory according to said operating sequence (See Column 3 Lines 32-33).

44. In reference to Claim 22, Hane discloses the limitations as applied to Claim 13 above. Hane further discloses that the data transferred between the interface and the mass storage memory is a navigation data base (See Column 8 Lines 35-60).

45. In reference to Claim 26, Hane discloses providing an add-on card (See Figure 1 Number 1) with a processing unit (See Figure 1 Number 10) and a non-volatile mass storage memory (See Figure 1 Number 11); causing the add-on card to be attached to the host system (See Column 5 Lines 8-14); processing data stored in the mass storage memory with the processing unit (See Column 3 Lines 32-33); and supplying the processed data to host (See Column 5 Lines 15-23).

46. In reference to Claim 31, Hane discloses the limitations as applied to Claim 26 above. Hane further discloses that the data stored in the mass storage memory is a navigation data base (See Column 8 Lines 35-60).

47. Claims 26, 27, and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 6,079,019 to Fukuzumi ("Fukuzumi-019").

48. In reference to Claim 26, Fukuzumi-019 discloses providing an add-on card (See Figure 5) with a processing unit (See Figure 5 Numbers 6 and 51) and a non-volatile mass storage memory (See Figure 5 Number 4); causing the add-on card to be attached to the host system (See Column 2 Lines 31-49); processing data stored in the mass storage memory with the processing unit (See Column 2 Lines 23-30); and supplying the processed data to host (See Column 2 Lines 11-30).

49. In reference to Claim 27, Fukuzumi-019 discloses the limitations as applied to Claim 26 above. Fukuzumi-019 further discloses that said processing is performed according to an application which at the host lacks (See Column 1 Line 64 – Column 2 Line 10).

50. In reference to Claim 28, Fukuzumi-019 discloses the limitations as applied to Claim 26 above. Fukuzumi-019 further discloses that the data stored in the mass storage memory is recorded prior to said causing the add-on card to be attached to the host system (See Column 2 Lines 23-30).

51. Claim 43 is rejected under 35 U.S.C. 102(b) as being anticipated by 6,038,551 to Barlow et al. ("Barlow").

52. In reference to Claim 43, Barlow discloses providing an add-on card (See Figure 3) including a processing unit (See Figure 3 Number 50) and a non-volatile mass storage memory (See Figure 3 Number 54), wherein the mass storage memory includes a program memory portion in which are stored a plurality of applications (See Figure 3 Number 66, Column 5 Lines 7-10, Column 10 Lines 55, and Column 11 Lines 49-52); coupling the add-on card to the host system (See Column 9 Lines 26-37); causing one of the applications to be selected (See Column 11 Lines 49-52 and Column 12 Lines 31-33); receiving data from the host on the add-on card (See Column 11 Lines 54-65); processing data received from the host with the processing unit according to the

selected application (See Column 12 Lines 31-35); and supplying the processed data to host (See Column 11 Lines 54-65).

53. In reference to Claim 44, Barlow discloses the limitations as applied to Claim 43 above. Barlow further discloses that the selected application is an application which the host lacks (See Column 5 Lines 4-11).

54. In reference to Claim 45, Barlow discloses the limitations as applied to Claim 43 above. Barlow further discloses that the data received from the host is continuous media (See Column 16 Lines 63-66).

55. In reference to Claim 48, Barlow discloses the limitations as applied to Claim 43 above. Barlow further discloses that the selected application is decryption (See Column 11 Lines 49-53).

56. In reference to Claim 49, Barlow discloses the limitations as applied to Claim 43 above. Barlow further discloses that the selected application is encryption (See Column 11 Lines 49-53).

57. Claims 51 and 55 are rejected under 35 U.S.C. 102(b) as being anticipated by Fukuzumi-019.

58. In reference to Claim 51, Fukuzumi-019 discloses coupling an add-on card to a first host system (See Figure 5), and while so coupled: transferring data from the first host to the card (See Column 2 Lines 31-49); processing the data from the first host according to a first application (See Column 2 Lines 41-49); and storing the data processed according to the first application on the card (See Column 2 Lines 41-45); decoupling the add-on card from the first host system. Fukuzumi-019 further discloses that the IC memory card complies with PC card standards (See Column 1 Lines 6-10), and as such is inherently capable of being disconnected from the first host system and coupled to a second host system. Fukuzumi-019 further discloses coupling the add-on card to a second host system, and while so coupled: transferring the stored data from the card to the second host (See Column 2 Lines 11-30); and processing the stored data according to a second application (See Column 2 Lines 23-30), wherein at least one of the hosts lacks the application according to which the processing while the card is attached to said at least one of the hosts is performed (See Column 1 Line 64 – Column 2 Line 10).

59. In reference to Claim 53, Fukuzumi-019 discloses the limitations as applied to Claim 51 above. Fukuzumi-019 further discloses that the first application is data encryption (See Column 2 Lines 23-30) and that the second application is data decryption (See Column 2 Lines 41-49).

60. Claims 54 and 55 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 6,047,342 to Depew et al. ("Depew").

61. In reference to Claim 54, Depew discloses providing an add-on card (See Figure 4 Number 340) with a processing unit (See Figure 4 Number 350), wherein a plurality of applications are stored in the combined host/card system (See Figure 3); coupling the add-on card to the host system (See Column 1 Lines 44-50); causing one of the applications to be selected (See Column 6 Lines 20-37); processing data according to the selected application, wherein said processing is performed by the card's processing unit and the host processing system together on an application level (See Column 6 Lines 30-37 and Column 7 Lines 43-54).

62. In reference to Claim 55, Depew discloses the limitations as applied to Claim 54 above. Depew further discloses that said processing comprises executing a plurality of tasks, and wherein at least one of the tasks is executed by the host processing system and at least one of the tasks is allocated by the host to be executed by the card's processing unit (See Column 6 Lines 20-29).

Claim Rejections - 35 USC § 103

63. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

64. Claims 5 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peyret and FOLDOC as applied to Claims 4 and 17 above, and further in view of US Patent Number 5,737,582 to Fukuzumi ("Fukuzumi-582").

65. In reference to Claim 5, Peyret and FOLDOC teach the limitations as applied to Claim 4 above. Peyret and FOLDOC do not teach a data cache memory connected to the processor and the mass storage memory for buffering the continuous media transferred between the card and the processing system. Fukuzumi-582 teaches an input/output buffer memory on an IC card for buffering data transmitted between a host device and a device on the card (See Column 14 Lines 3-6).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Peyret and FOLDOC using the buffer of Fukuzumi-582, resulting in the invention of Claim 5, in order to allow a correction of any delay of the communication rate taking place between the host system and the

connected device, and thus allow the host system and the device to operate at different speeds (See Column 14 Lines 3-6).

66. In reference to Claim 18, Peyret and FOLDOC teach the limitations as applied to Claim 17 above. Peyret further discloses that the mass storage is a flash memory (See Column 4 Lines 63-67) which is a non-linear memory. Thus, data is inherently stored non-linearly. Peyret and FOLDOC do not teach a data cache memory connected to the processor and the mass storage memory for buffering the data transferred between the interface and the mass storage memory. Fukuzumi-582 teaches an input/output buffer memory on an IC card for buffering data transmitted between a host device and a device on the card (See Column 14 Lines 3-6).

67. It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Peyret and FOLDOC using the buffer of Fukuzumi-582, resulting in the invention of Claim 18, in order to allow a correction of any delay of the communication rate taking place between the host system and the connected device, and thus allow the host system and the device to operate at different speeds (See Column 14 Lines 3-6).

68. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peyret as applied to Claim 1 above, and further in view of US Patent Number 6,266,671 to Niimura ("Niimura").

69. In reference to Claim 6, Peyret teaches the limitations as applied to Claim 1 above. Peyret does not teach that said at least one additional operation sequence includes a decompression program. Niimura teaches a PC card memory device which is capable of compressing data received from a host device for storage in a memory and decompressing data stored in the memory for transmission to the host device (See Figure 1 and Column 2 Lines 49-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Peyret and FOLDOC with the data compression and decompression ability of Niimura, resulting in the invention of Claim 6, in order to increase the storage capacity of the memory and fit as much data as possible into the available storage space (See Column 1 Lines 25-28 of Niimura).

70. In reference to Claim 7, Peyret teach the limitations as applied to Claim 1 above. Peyret does not teach that said at least one operation sequence includes a compression program. Niimura teaches a PC card memory device which is capable of compressing data received from a host device for storage in a memory and decompressing data stored in the memory for transmission to the host device (See Figure 1 and Column 2 Lines 49-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Peyret with the data compression and decompression ability of Niimura, resulting in the invention of Claim 7, in order to

increase the storage capacity of the memory and fit as much data as possible into the available storage space (See Column 1 Lines 25-28 of Niimura).

71. Claims 9 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peyret as applied to Claim 1 above, and further in view of Dunn.

72. In reference to Claim 9, Peyret teaches the limitations as applied to Claim 1 above. Peyret does not teach that at least one additional operating sequence includes a voice-recognition program. Dunn teaches a smart card which receives voice recognition information from the host for processing (See Column 6 Lines 8-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Peyret with the voice-recognition processing of Dunn, resulting in the invention of Claim 9, in order to improve overall security by limiting accessibility to secure information and security processes.

73. In reference to Claim 24, Peyret teaches the limitations as applied to Claim 13 above. Peyret does not teach that said at least one operating sequence includes a voice-recognition program. Dunn teaches a smart card which receives voice recognition information from the host for processing (See Column 6 Lines 8-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Peyret with the voice-recognition

processing of Dunn, resulting in the invention of Claim 24, in order to improve overall security by limiting accessibility to secure information and security processes.

74. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peyret and FOLDOC as applied to Claim 17 above, and further in view of Niimura.

75. In reference to Claim 20, Peyret and FOLDOC teach the limitations as applied to Claim 17 above. Peyret and FOLDOC do not teach that said at least one operation sequence includes a decompression program. Niimura teaches a PC card memory device which is capable of compressing data received from a host device for storage in a memory and decompressing data stored in the memory for transmission to the host device (See Figure 1 and Column 2 Lines 49-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Peyret and FOLDOC with the data compression and decompression ability of Niimura, resulting in the invention of Claim 20, in order to increase the storage capacity of the memory and fit as much data as possible into the available storage space (See Column 1 Lines 25-28 of Niimura).

76. In reference to Claim 21, Peyret and FOLDOC teach the limitations as applied to Claim 17 above. Peyret and FOLDOC do not teach that said at least one operation sequence includes a compression program. Niimura teaches a PC card memory device which is capable of compressing data received from a host device for storage in a

memory and decompressing data stored in the memory for transmission to the host device (See Figure 1 and Column 2 Lines 49-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Peyret and FOLDOC with the data compression and decompression ability of Niimura, resulting in the invention of Claim 21, in order to increase the storage capacity of the memory and fit as much data as possible into the available storage space (See Column 1 Lines 25-28 of Niimura).

77. Claims 26 27, 29, 30, 32, 33, 36, 37, 38, 39, 40, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Depew and US Patent Number 6,097,618 to Jenne ("Jenne").

78. In reference to Claim 26, Depew teaches providing an add-on card (See Figure 4 Number 340) with a processing unit (See Figure 4 Number 350) and a mass storage memory (See Figure 4 Number 354); causing the add-on card to be attached to the host system (See Column 1 Lines 44-50); processing data stored in the mass storage memory with the processing unit (See Column 7 Lines 43-54); and supplying the processed data to host (See Column 7 Line 61 – Column 8 Line 7). Depew does not teach that the mass storage memory is non-volatile. Jenne teaches the use of a non-volatile RAM (See Column 2 Lines 20-34).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the add-on card of Depew with the non-volatile RAM of

Jenne, resulting in the invention of Claim 26, in order to provide fault tolerance by preventing a loss of the information stored in the memory when power is removed or temporarily lost (See Column 1 Lines 23-26 and Column 2 Lines 3-9 of Jenne).

79. In reference to Claim 27, Depew and Jenne teach the limitations as applied to Claim 26 above. Depew further teaches that the processing is performed according to an application which the host lacks (See Column 2 Line 58 – Column 3 Line 22).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the add-on card of Depew with the non-volatile RAM of Jenne, resulting in the invention of Claim 27, in order to provide fault tolerance by preventing a loss of the information stored in the memory when power is removed or temporarily lost (See Column 1 Lines 23-26 and Column 2 Lines 3-9 of Jenne).

80. In reference to Claim 29, Depew and Jenne teach the limitations as applied to Claim 26 above. Depew further teaches that the data stored in the mass storage memory is continuous media (See Column 7 Lines 43-54).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the add-on card of Depew with the non-volatile RAM of Jenne, resulting in the invention of Claim 29, in order to provide fault tolerance by preventing a loss of the information stored in the memory when power is removed or temporarily lost (See Column 1 Lines 23-26 and Column 2 Lines 3-9 of Jenne).

81. In reference to Claim 30, Depew and Jenne teach the limitations as applied to Claim 29 above. Depew further teaches that data stored in the mass storage memory is stored in compressed form, and wherein said processing is decompressing (See Column 7 Line 43 – Column 8 Line 15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the add-on card of Depew with the non-volatile RAM of Jenne, resulting in the invention of Claim 30, in order to provide fault tolerance by preventing a loss of the information stored in the memory when power is removed or temporarily lost (See Column 1 Lines 23-26 and Column 2 Lines 3-9 of Jenne).

82. In reference to Claim 32, Depew and Jenne teach the limitations as applied to Claim 26 above. Depew further teaches that data stored in the mass storage memory is stored in encrypted form, and wherein said processing is decrypting (See Column 7 Lines 2-7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the add-on card of Depew with the non-volatile RAM of Jenne, resulting in the invention of Claim 32, in order to provide fault tolerance by preventing a loss of the information stored in the memory when power is removed or temporarily lost (See Column 1 Lines 23-26 and Column 2 Lines 3-9 of Jenne).

83. In reference to Claim 33, Depew and Jenne teach the limitations as applied to Claim 26 above. Depew further teaches that a plurality of applications are stored on the

add-on card, and causing the selection an application from the plurality of applications, wherein said processing is performed according to the selected application (See Column 10 Lines 32-38).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the add-on card of Depew with the non-volatile RAM of Jenne, resulting in the invention of Claim 33, in order to provide fault tolerance by preventing a loss of the information stored in the memory when power is removed or temporarily lost (See Column 1 Lines 23-26 and Column 2 Lines 3-9 of Jenne).

84. In reference to Claim 35, Depew and Jenne teach the limitations as applied to Claim 26 above. Depew further teaches that subsequent to causing the add-on card to be attached to the host system and prior to processing data stored in the mass storage memory with the processing unit: providing data from the host to the add-on card (See Column 7 Lines 43-54); processing the data provided from the host with the processing unit (See Column 7 Lines 43-54); and storing in the mass storage memory the data from the host processed with the processing unit (See Column 7 Lines 62-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the add-on card of Depew with the non-volatile RAM of Jenne, resulting in the invention of Claim 35, in order to provide fault tolerance by preventing a loss of the information stored in the memory when power is removed or temporarily lost (See Column 1 Lines 23-26 and Column 2 Lines 3-9 of Jenne).

85. In reference to Claim 36, Depew teaches providing an add-on card (See Figure 4 Number 340) with a processing unit (See Figure 4 Number 350) and a mass storage memory (See Figure 4 Number 354); causing the add-on card to be attached to the host system (See Column 1 Lines 44-50); supplying data from the host to the add-on card (See Column 7 Lines 43-54); processing data supplied from the host with the processing unit (See Column 7 Lines 43-54); and storing the processed data in the mass storage memory (See Column 7 Lines 62-67). Depew does not teach that the mass storage memory is non-volatile. Jenne teaches the use of a non-volatile RAM (See Column 2 Lines 20-34).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the add-on card of Depew with the non-volatile RAM of Jenne, resulting in the invention of Claim 36, in order to provide fault tolerance by preventing a loss of the information stored in the memory when power is removed or temporarily lost (See Column 1 Lines 23-26 and Column 2 Lines 3-9 of Jenne).

86. In reference to Claim 37, Depew and Jenne teach the limitations as applied to Claim 36 above. Depew further teaches that the processing is performed according to an application which the host lacks (See Column 2 Line 58 – Column 3 Line 22).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the add-on card of Depew with the non-volatile RAM of Jenne, resulting in the invention of Claim 37, in order to provide fault tolerance by

preventing a loss of the information stored in the memory when power is removed or temporarily lost (See Column 1 Lines 23-26 and Column 2 Lines 3-9 of Jenne).

87. In reference to Claim 38, Depew and Jenne teach the limitations as applied to Claim 36 above. Depew further teaches that the data stored in the mass storage memory is continuous media (See Column 7 Lines 43-54).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the add-on card of Depew with the non-volatile RAM of Jenne, resulting in the invention of Claim 38, in order to provide fault tolerance by preventing a loss of the information stored in the memory when power is removed or temporarily lost (See Column 1 Lines 23-26 and Column 2 Lines 3-9 of Jenne).

88. In reference to Claim 39, Depew and Jenne teach the limitations as applied to Claim 38 above. Depew further teaches that data stored in the mass storage memory is stored in compressed form, and wherein said processing is decompressing (See Column 7 Line 43 – Column 8 Line 15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the add-on card of Depew with the non-volatile RAM of Jenne, resulting in the invention of Claim 39, in order to provide fault tolerance by preventing a loss of the information stored in the memory when power is removed or temporarily lost (See Column 1 Lines 23-26 and Column 2 Lines 3-9 of Jenne).

89. In reference to Claim 40, Depew and Jenne teach the limitations as applied to Claim 36 above. Depew further teaches that data stored in the mass storage memory is stored in encrypted form, and wherein said processing is decrypting (See Column 7 Lines 2-7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the add-on card of Depew with the non-volatile RAM of Jenne, resulting in the invention of Claim 32, in order to provide fault tolerance by preventing a loss of the information stored in the memory when power is removed or temporarily lost (See Column 1 Lines 23-26 and Column 2 Lines 3-9 of Jenne).

90. In reference to Claim 41, Depew and Jenne teach the limitations as applied to Claim 36 above. Depew further teaches that a plurality of applications are stored on the add-on card, and causing the selection an application from the plurality of applications, wherein said processing is performed according to the selected application (See Column 10 Lines 32-38).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the add-on card of Depew with the non-volatile RAM of Jenne, resulting in the invention of Claim 41, in order to provide fault tolerance by preventing a loss of the information stored in the memory when power is removed or temporarily lost (See Column 1 Lines 23-26 and Column 2 Lines 3-9 of Jenne).

91. In reference to Claim 35, Depew and Jenne teach the limitations as applied to Claim 26 above. Depew further teaches that subsequent to causing the add-on card to be attached to the host system and prior to processing data stored in the mass storage memory with the processing unit: providing data from the host to the add-on card (See Column 7 Lines 43-54); processing the data provided from the host with the processing unit (See Column 7 Lines 43-54); and storing in the mass storage memory the data from the host processed with the processing unit (See Column 7 Lines 62-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the add-on card of Depew with the non-volatile RAM of Jenne, resulting in the invention of Claim 35, in order to provide fault tolerance by preventing a loss of the information stored in the memory when power is removed or temporarily lost (See Column 1 Lines 23-26 and Column 2 Lines 3-9 of Jenne).

92. Claims 46 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barlow as applied to Claim 45 above, and further in view of Niimura.

93. In reference to Claim 46, Barlow teaches the limitations as applied to Claim 45 above. Barlow does not teach that the selected application is data decompression. Niimura teaches a PC card memory device which is capable of compressing data received from a host device for storage in a memory and decompressing data stored in the memory for transmission to the host device (See Figure 1 and Column 2 Lines 49-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the IC card of Barlow with the data compression and decompression ability of Niimura, resulting in the invention of Claim 46, in order to increase the storage capacity of the memory card and fit as much data as possible into the available storage space (See Column 1 Lines 25-28 of Niimura).

94. In reference to Claim 46, Barlow teaches the limitations as applied to Claim 45 above. Barlow does not teach that the selected application is data compression. Niimura teaches a PC card memory device which is capable of compressing data received from a host device for storage in a memory and decompressing data stored in the memory for transmission to the host device (See Figure 1 and Column 2 Lines 49-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the IC card of Barlow with the data compression and decompression ability of Niimura, resulting in the invention of Claim 46, in order to increase the storage capacity of the memory card and fit as much data as possible into the available storage space (See Column 1 Lines 25-28 of Niimura).

95. Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over Barlow as applied to Claim 43 above, and further in view of Dunn.

96. In reference to Claim 50, Barlow teaches the limitations as applied to Claim 43 above. Barlow does not teach that at least one additionally operating sequence includes a voice-recognition program. Dunn teaches a smart card which receives voice recognition information from the host for processing (See Column 6 Lines 8-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Barlow with the voice-recognition processing of Dunn, resulting in the invention of Claim 50, in order to improve overall security by limiting accessibility to secure information and security processes.

97. Claim 52 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuzumi-019 as applied to Claim 51 above, and further in view of Niimura.

98. In reference to Claim 52, Fukuzumi-019 teaches the limitations as applied to Claim 51 above. Fukuzumi-019 does not teach that the first application is data compression and the second application is data decompression. Niimura teaches a PC card memory device which is capable of compressing data received from a host device for storage in a memory and decompressing data stored in the memory for transmission to the host device (See Figure 1 and Column 2 Lines 49-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the PC card of Fukuzumi-019 with the data compression and decompression ability of Niimura, resulting in the invention of Claim

51, in order to increase the storage capacity of the memory card and fit as much data as possible into the available storage space (See Column 1 Lines 25-28 of Niimura).

Drawings

99. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations of Independent Claim 51 and dependent Claims 52 and 53 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will

be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

100. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the Examiner, the Applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The examiner can normally be reached on Monday-Thursday (7-3:30), Alt. Fridays (7-2:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

TJC

Thomas J. Cleary
Patent Examiner
Art Unit 2111